IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Alan L. Renninger et al. PATENT APPLICATION
Serial No.: 10/717,149 Group Art Unit: 2818
Filed: November 18, 2003 Examiner: D.A. Le
For: METHOD OF FORMING A LOW VOLTAGE GATE OXIDE LAYER AND TUNNEL OXIDE LAYER IN AN EEPROM CELL (as amended)

Amendment

Hon. Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office action mailed July 15, 2004, from the Patent and Trademark Office regarding the above-identified patent application, please amend the above referenced application as follows.

In the Drawings:

Figure 2C has been amended to improve the consistency with Figures 3A and 3B. In Figure 2C, the LOGIC GATES and EEPROM CELL drawings have been switched or reversed and the LV logic gate area has been amended to better correspond with the cross-sectional views in Figures 3A and 3B.

Figures 2B, 3A (ii), and 3B (ii) have been amended for clarity. In Figure 2B, reference number 86 still refers to the same area of the drawing, but has been moved for clarity. In Figure 3A (vi), reference 67 has been added.

The amended drawings are enclosed. Amended items are circled in red on the enclosed copies of marked-up drawings. Also enclosed are new formal drawings incorporating the amendments.

Applicants respectfully request that the new formal drawings be entered and that no new matter has been added.

In the Title:

Please replace the title with:

METHOD OF FORMING A LOW VOLTAGE GATE OXIDE LAYER AND TUNNEL OXIDE LAYER IN AN EEPROM CELL